Aim: The aim of this experiment is NMOS and PMOS Characteristics (transfer and output characteristics) and analysis using Cadence simulation software

**Tools Used**: Cadence Software

### Pmos

**1. Transfer Characteristics:**

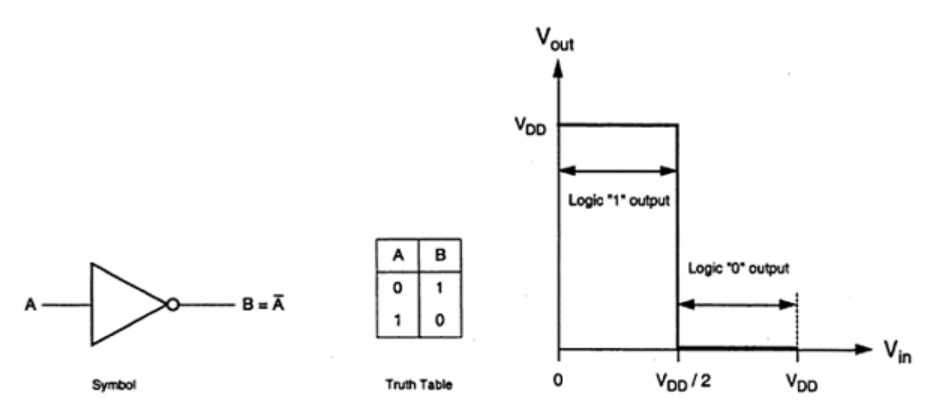
For a PMOS transistor, the drain current IDI\_DID​ in the saturation region is:

where:

* Vsg​ is the source-gate voltage.
* ∣Vth∣ is the magnitude of the threshold voltage.

2. Output Characteristics:

In the saturation region, the output characteristics for the PMOS transistor are:



ϕ(f)=−arctan(2πfRC)

### circuit Design

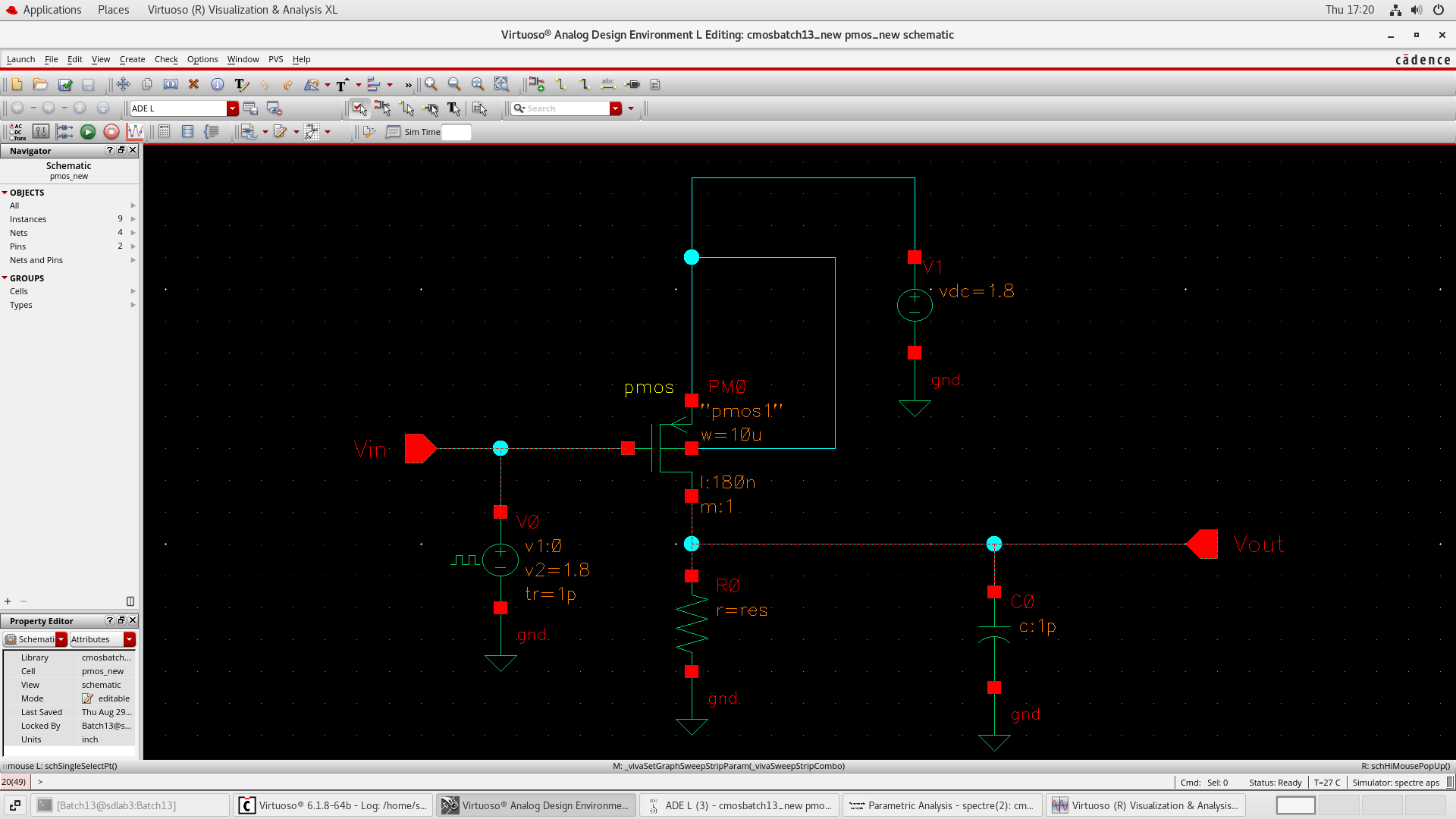


Fig: Circuit Diagram PMOS Inverter

* **Transfer Characteristics**

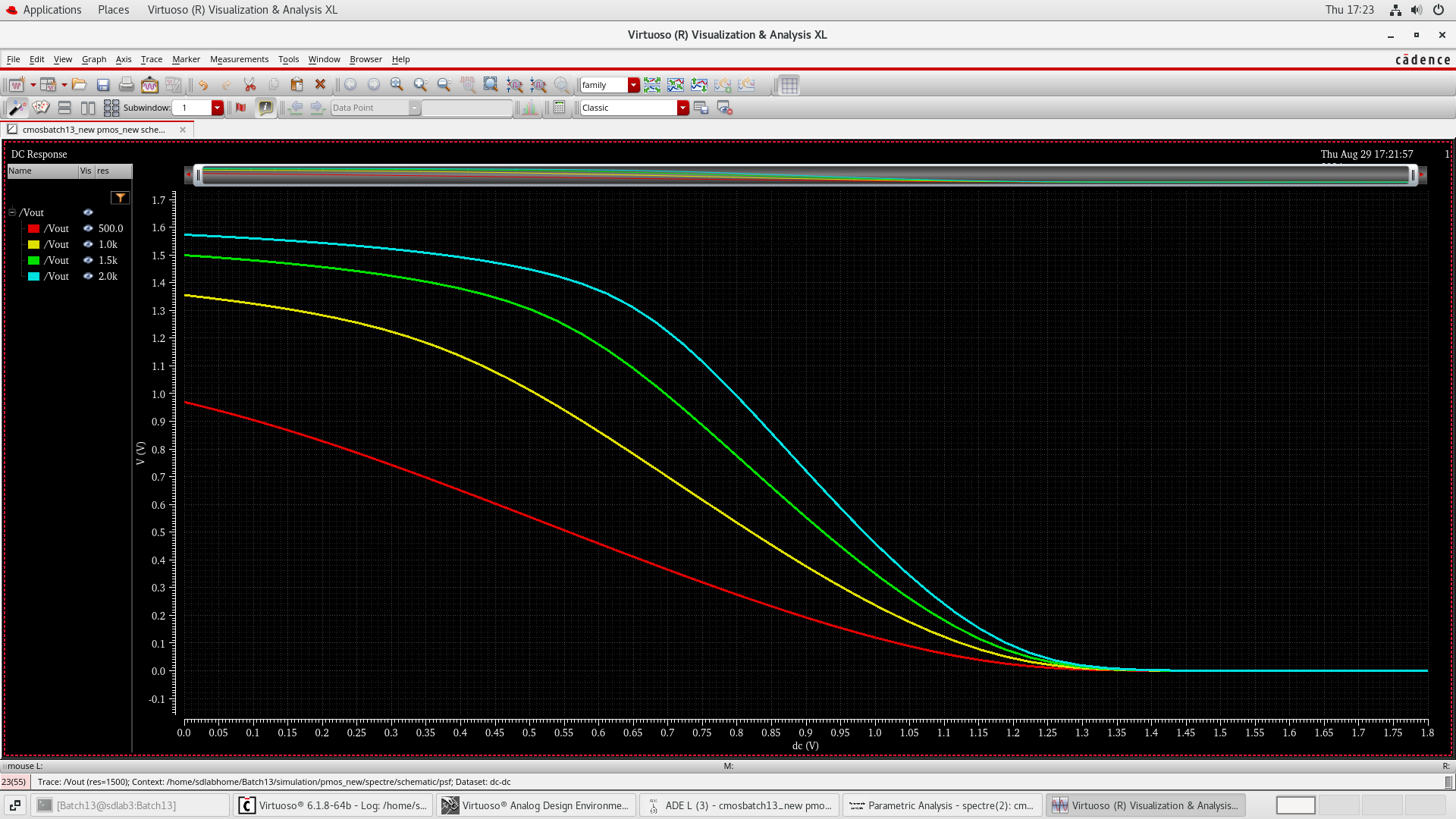


Fig: Parametric Analysis Vin vs Vout for different values of load resistance (NMOS)

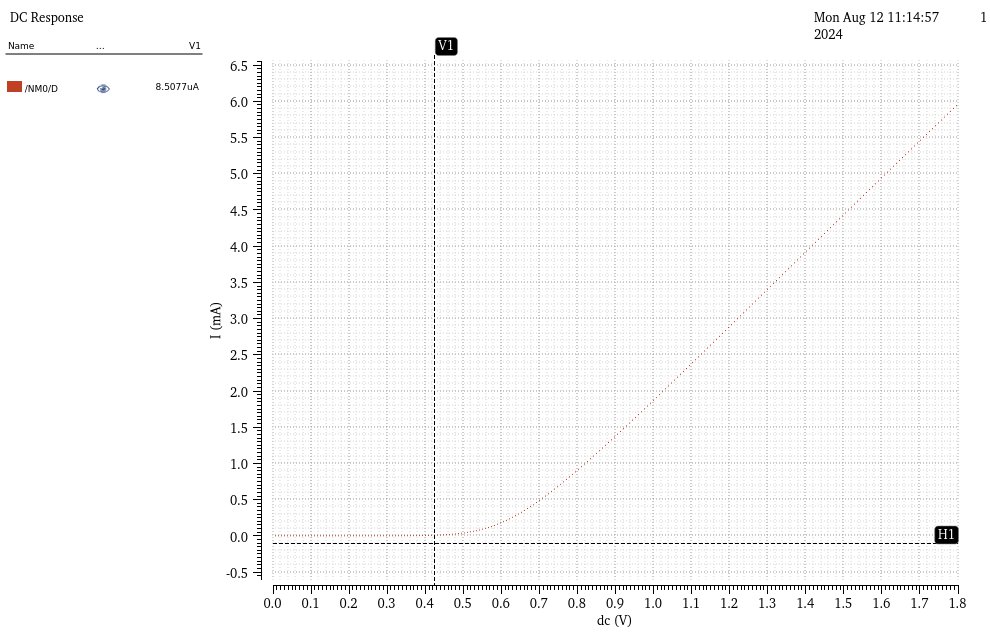


Fig: Id​ versus Vgs for different vds ( NMOS)

1. **PMOS:**

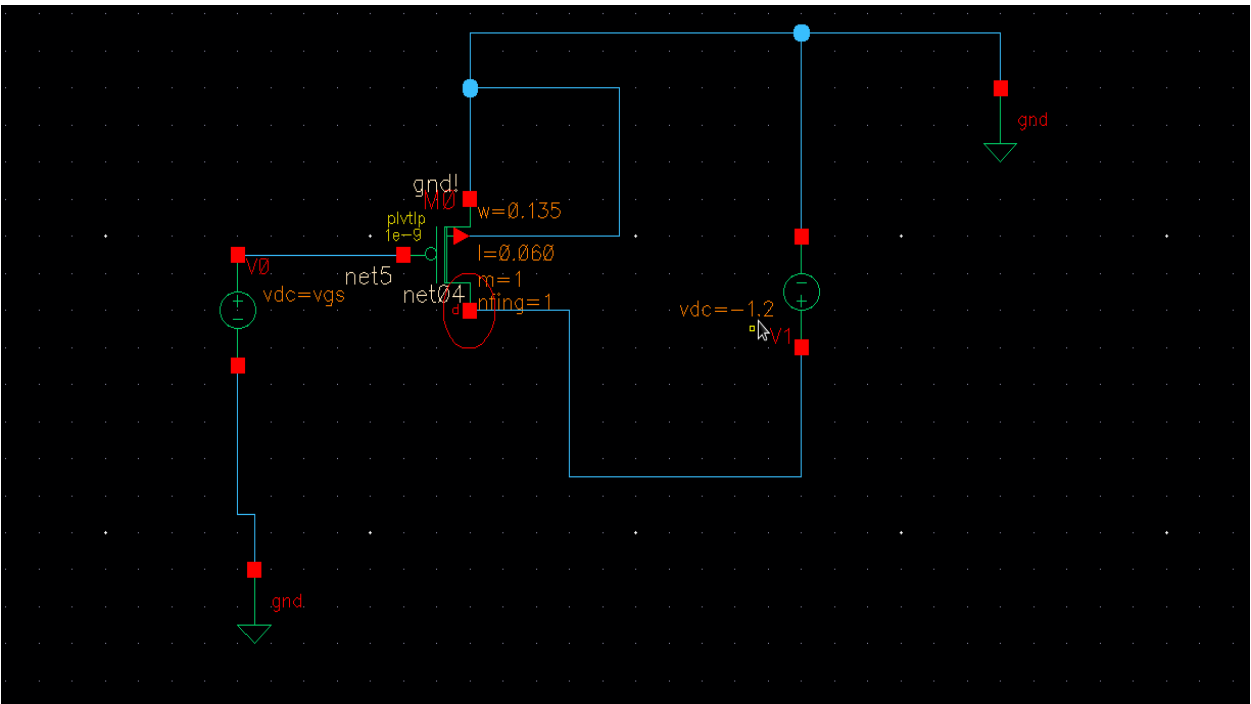


Fig: Circuit Diagram PMOS

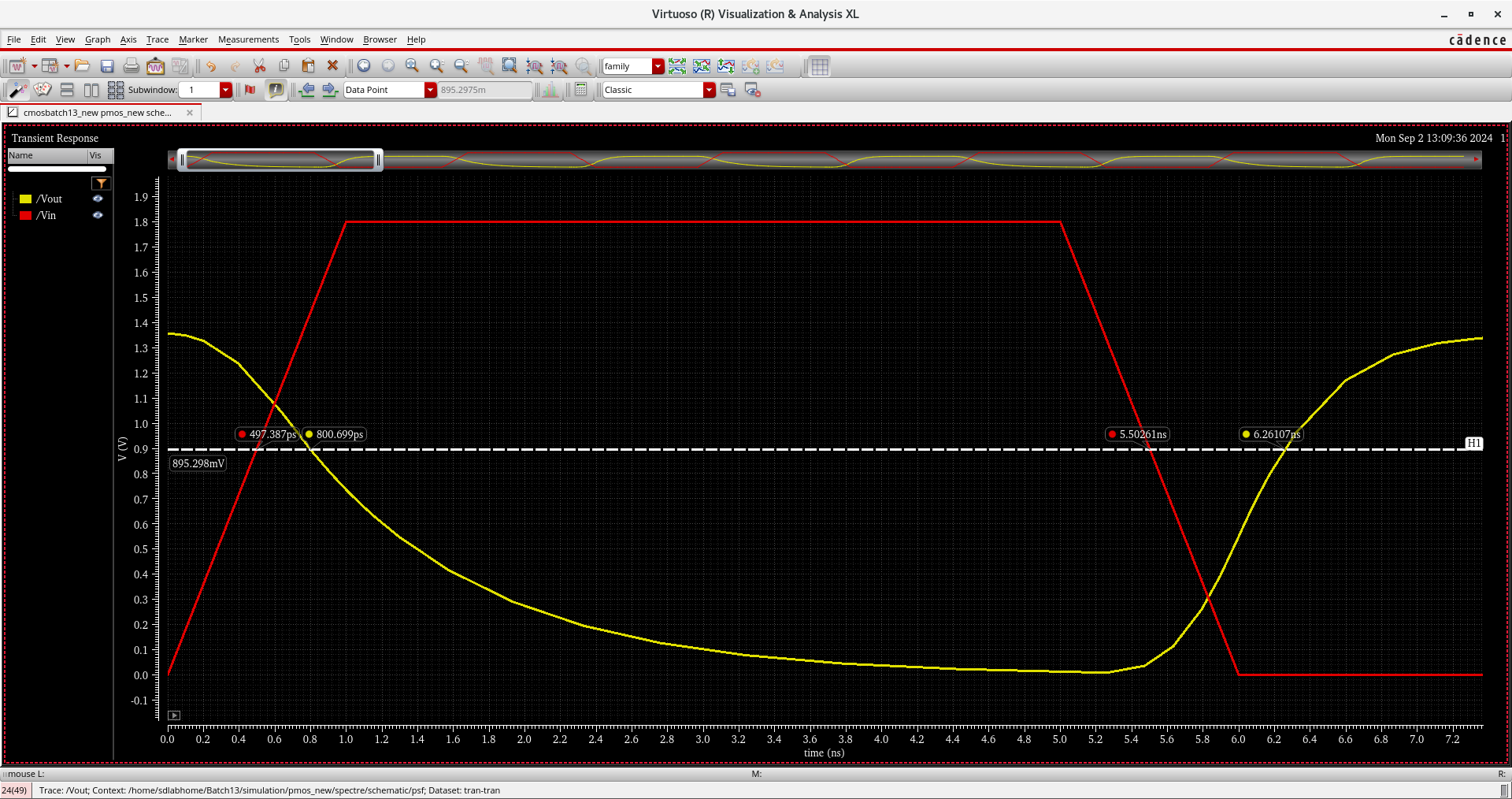


Fig: Transient response

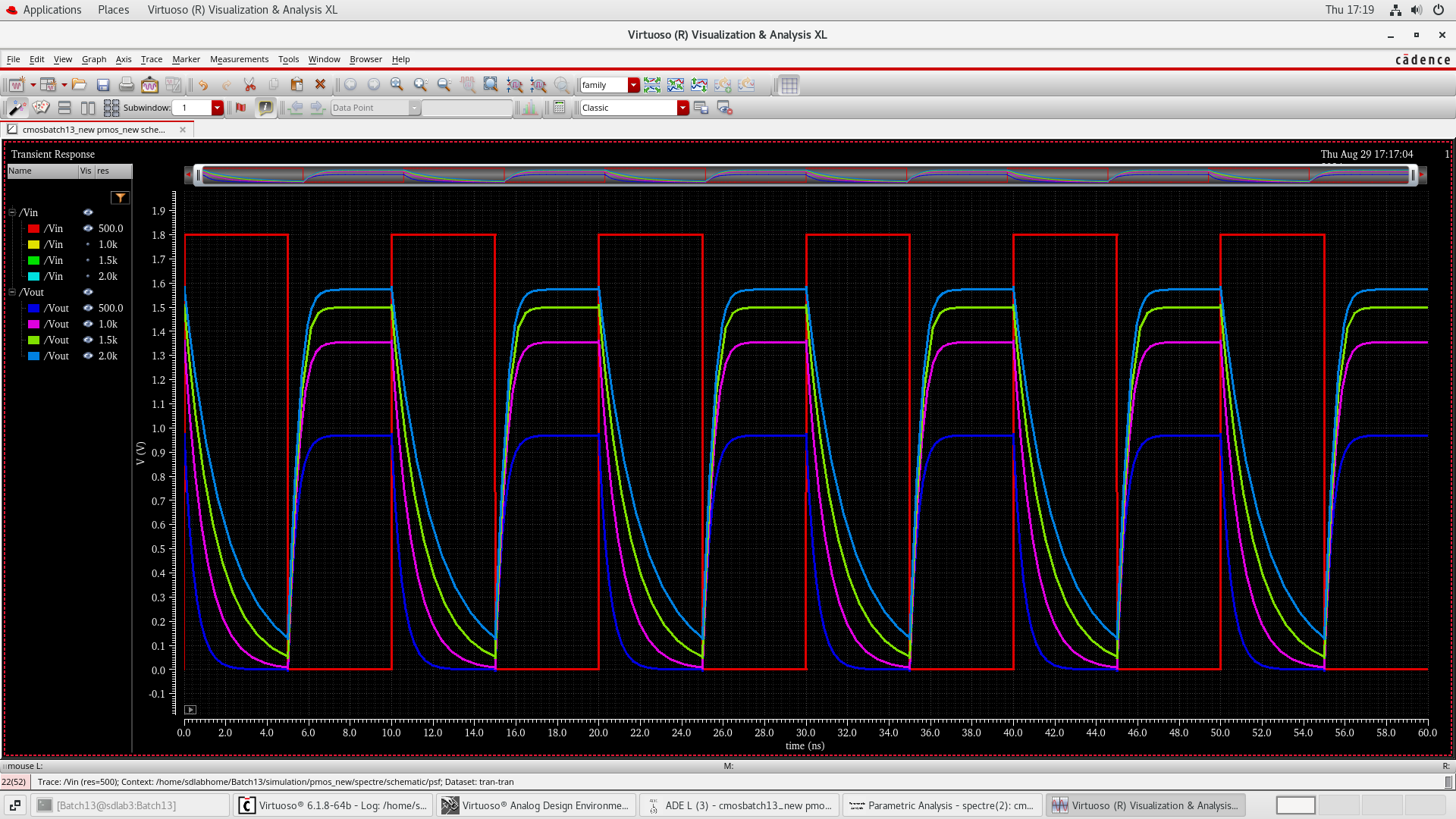


Fig: Circuit response for multiple values of resistane

### procedure

**1. Setup in Cadence:**

1. Open Cadence Virtuoso and create a new schematic for the PMOS inverter circuits.
2. Add an PMOS transistor and a DC voltage source for VGS​ and VDS​.
3. Connect the drain of the PMOS transistor to the output node
4. Attach a load resistor RL=10kΩ between Vout and ground
5. Connect a load capacitance Cl = 10pf at the output node to model the capacitive load
6. Connect the measurement probes to record the drain current Id and the gate voltage Vgs or Vsg​.

**2. Simulation of Transfer Characteristics:**

1. Set Vds​ to a constant value (e.g., 0 to 1.8V).
2. Measure and record the corresponding Vout ​ values to plot the transfer characteristics
3. Run the simulation and plot Id versus Vgs​ to obtain the transfer characteristics.

**3. Simulation of Propagation Delay:**

1. Apply a input to Vin and perform transient analysis.
2. Measure the time taken for Vout to transition form 50% of its intial value to 50% of its final value

**4. Power Dissipation calculation:**

1. Calculate dynamic power dissipation using the specified frequency f = 387.7 MHz

### Observations

1. **Transfer Characteristics:**
   * The Vout ​ remains high (close to VDD) when Vin​ is low (near 0V), indicating the PMOS transistor is conducting.
   * As Vin​ increases, Vout begins to decrease, reflecting the PMOS transistor transitioning towards the cutoff region.
   * A sharp transition in Vout occurs around the threshold voltage Vth=−0.4V, demonstrating effective switching behavior.
2. **Propagation Delay:**
   * The propagation delay tpt\_ptp​ was measured at the 50% transition point of the input and output voltages.
   * Rise time (tpLH ​) and fall time (tpHL​) were consistent with theoretical predictions, each contributing approximately 3.47 ns to the total delay.
   * The total propagation delay tp was calculated to be approximately 6.94 ns.
3. **Power Dissipation:**
   * Dynamic power dissipation was calculated without considering leakage currents.
   * At a switching frequency of 387.7 MHz, the dynamic power dissipation was determined to be approximately 1.25 mW.
   * The power dissipation is directly proportional to the load capacitance CL and the switching frequency f.
4. **Overall Performance:**
   * The PMOS inverter exhibited a sharp and well-defined transition in the transfer characteristics, essential for reliable digital logic operations.
   * The propagation delay was minimal, indicating the inverter's suitability for high-speed applications.
   * Power dissipation remained within acceptable limits for low-power digital circuits.

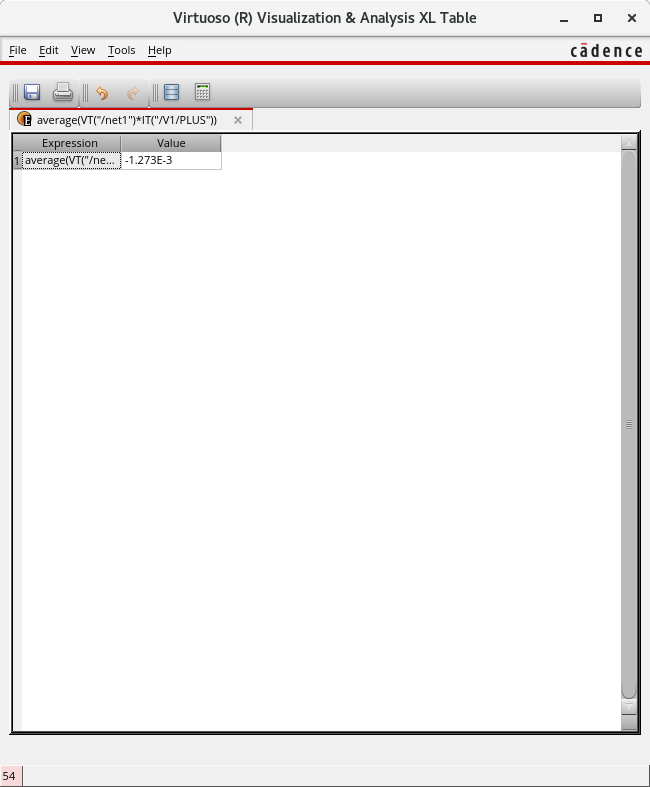
### Results

**1.Transfer Characteristics**

The transfer characteristics plot (Vout​ vs Vin​) reveals the following:

* **Low Input Voltage (Vin​ < Vth):**
  + PMOS transistor is on.
  + Vout​ is high, close to VDD=1.8V .
* **High Input Voltage (Vin ​ > Vth):**
  + PMOS transistor is off.
  + Vout is low, approaching 0V.
* **Transition Region:**
  + Sharp change in Vout​ occurs around Vth=−0.4V.

**2. Power Dissipation Calculation**



### conclusion

The following observations were made: Transfer Characteristics:

The Vout ​ remains high (close to VDD ​ ) when Vin ​ is low (near 0V), indicating the PMOS transistor is conducting. As Vin ​ increases, Vout ​ begins to decrease, reflecting the PMOS transistor transitioning towards the cutoff region. A sharp transition in Vout ​ occurs around the threshold voltage Vth ​ = −0.4V, demonstrating effective switching behavior. Propagation Delay: The propagation delay tp ​ was measured at the 50% transition point of the input and output voltages. Rise time (tpLH) and fall time (tpHL) were consistent with theoretical predictions, each contributing approximately 3.47 ns to the total delay.

The total propagation delay tp ​ was calculated to be approximately 6.94 ns.

Power Dissipation: Dynamic power dissipation was calculated. At a switching frequency of 387.7 MHz, the dynamic power dissipation was determined to be approximately 1.25 mW. The power dissipation is directly proportional to the load capacitance CL ​ and the switching frequency 𝑓 f.

Overall Performance: The PMOS inverter exhibited a sharp and well-defined transition in the transfer characteristics, essential for reliable digital logic operations. The propagation delay was minimal, indicating the inverter's suitability for high-speed applications. Power dissipation remained within acceptable limits for low-power digital circuits.